

11 supported by the set of low-level instructions, the set of low-level
12 instructions to ensure atomicity of the memory update operation.

1 21. The machine-readable medium of claim 20 wherein the set of low-level
2 instructions encapsulate the memory update operation.

1 22. The machine-readable medium of claim 20 further comprising translating the first
2 program unit into a third program unit upon determining that a second set of one or more
3 low-level instructions support the memory update operation for the data-type and the data
4 size of the operand, the second set of low-level instructions for performing the memory
5 update operation atomically.

1 23. The machine-readable medium of claim 20 further comprising translating the first
2 program unit into a third program unit upon determining that a second set of low-level
3 instructions does not support the memory update operation for the data-type and the data
4 size of the operand and that the set of low-level instructions does not support the data size
5 of the operand, the third program unit to associate the memory update operation with a set
6 of locking instructions.

1 24. The machine-readable medium of claim 20 wherein the set of low-level
2 instructions for ensuring atomicity is a compare-and-swap instruction.

1 25. A machine-readable medium that provides instructions, which when executed by a
2 set of one or more processors, cause said set of processors to perform operations
3 comprising:
4 receiving a first program unit, the first program unit including a memory update
5 operation to be performed atomically, the memory update operation
6 indicating an operand and an operator, the operand being of a data-type
7 and a data size;
8 translating the first program unit into a second program unit upon determining that
9 a first set of one or more low-level instructions support the memory update
10 operation for the data-type and the data size of the operand, the first set of
11 low-level instructions for performing the memory update operation
12 atomically;
13 translating the first program unit into a third program unit, the third program unit
14 to associate the memory update operation with a second set of one or more
15 low-level instructions upon determining that the data size of the operand is
16 supported by the second set of low-level instructions, the second set of
17 low-level instructions to ensure atomicity of the memory update operation;
18 and
19 translating the first program unit into a fourth program unit upon determining that
20 the first set of low-level instructions does not support the memory update
21 operation for the data-type and the data size of the operand and that the
22 second set of low-level instructions does not support the data size of the
23 operand, the fourth program unit to associate the memory update operation
24 with a set of locking instructions.

1 26. The machine-readable medium of claim 25 wherein the second set of low-level
2 instructions encapsulate the memory update operation.

1 27. The machine-readable medium of claim 25 wherein associating the second set of
2 instructions to the memory update operation comprises:
3 enclosing the memory update operation in a callback routine; and
4 referencing the callback routine from a routine that references the second set of low-level
5 instructions.

1 28. The machine-readable medium of claim 25 wherein the second set of low-level
2 instructions is a compare-and-swap instruction.

1 29. The machine-readable medium of claim 25 wherein the second set of low-level
2 instructions is a test-and-set instruction.